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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,415	02/05/2002	Ji Ung Lee	MI30-068	5182

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EXAMINER
YEVSIKOV, VICTOR V

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,415	LEE ET AL.	
	Examiner	Art Unit	
	Victor V Yevsikov	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *74-111* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *79-82,93-95 and 102-111* is/are allowed.

6)☒ Claim(s) *74-76,78,83-85,88-92 and 97-101* is/are rejected.

7)☒ Claim(s) *77,86,87 and 96* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/05/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 74, 75, 78, 83 – 85, 88 - 92 and are rejected under 35 U.S.C. 102(b) as being anticipated by Kanemaru et al. (U.S. 5,710,478).

With respect to claims 74, 75 and 78 Kanemaru teach a method of fabrication field effect transistor, wherein:

a semiconductive material 11 including a channel region 23,

a source semiconductive region 21 and a drain semiconductive region 22 adjacent to the channel region 23, and wherein the drain region 22 comprises providing an emitter;

a gate dielectric material 24 over the channel region 23, and

a gate 25 over the gate dielectric material 24 and the channel region 23; and wherein:

75. the semiconductive material comprises a thin film semiconductive layer.

78. the gate comprises providing the gate about the emitter.

With respect to claims 83 - 85 and 88 Kanemaru teach a method of fabrication a field emission device, wherein:

semiconductive material 11;

a plurality of semiconductive regions 21,22 adjacent to the semiconductive material, and wherein the providing the semiconductive regions comprises providing one of the regions 22 comprising an emitter 11; and

a gate 25 intermediate the semiconductive regions;

84. the thin film semiconductive layer 11;

85. the semiconductive regions and the gate 14 comprise forming a field effect transistor;

88. the gate comprises the gate 14 about the emitter 13.

With respect to claims 89-92 Kanemaru teach a method of fabrication a field emission device, wherein:

a plurality of semiconductive regions adjacent to a channel region, and the semiconductive regions comprises an emitter; and

controlling current flow intermediate the semiconductive regions within the channel region and controlling emission of electrons from the field emitter using a gate intermediate the semiconductive regions;

90. the semiconductive regions adjacent to semiconductive regions comprises material comprising a semiconductive layer;

91. the semiconductive regions adjacent to semiconductive material comprising a thin film semiconductive layer;

92. (New) The method of claim 89 further comprising configuring the gate and the semiconductive regions to form a field effect transistor.

Reference: figs. 1, 6A-7B; col1-3, lines 29-40; col.5, lines 38-42; cols. 6-8, lines 19-32.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 76 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanemaru in view of Inaba (US 6,329,258 B1).

Kanemaru teaches the features detailed previously but lacks a discussion on the method, wherein the gate comprises polishing the gate dielectric material and gate material to form the gate aligned with the channel region of the semiconductive material.

However, Inaba teaches the method wherein the gate comprises polishing the gate dielectric material and gate material to form the gate aligned with the channel region of the semiconductive material (figs. 8B and 8D; col.13, lines 32-47). The etching to make the gate/gate dielectric will align the gate/gate dielectric with channel.

Therefore, it would have been obvious to one of ordinary skill in the art to use method of polishing to form the gate aligned with channel region as taught by Kanemaru /Inaba as is useful in the fabrication of microelectronic devices.

Claims 97-101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanemaru in view of Inaba and in view of Gardner et al. (US 6,140,167).

Kanemaru/ Inaba teaches the features detailed previously but lacks a discussion on the method, wherein the gate aligning with the channel region using the gate dielectric layer.

However, Gardner teaches the method wherein the gate aligning with the channel region using the gate dielectric layer (col. 1, lines 18-29).

Therefore, it would have been obvious to one of ordinary skill in the art method of the gate aligning as taught by Kanemaru /Inaba/Gardner for fabrication field effect transistor device.

Claim Objections

Claims 77, 86, 87 and 96 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

Claims 79-82, 93-95 and 102-111 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art does not teach a method wherein self-aligning a gate with the semi conductive regions after the providing the semiconductive regions.

Further, prior art does not teach a method wherein a gate comprising gate material over the channel region of the semiconductive material without the use of a mask over the gate material;

Also, prior art does not teach a method of polishing the gate dielectric material and the gate material to form a gate over the channel region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Yevsikov

Victor Yevsikov
Examiner
Art Unit 2825

December 8, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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